

Amendments to the claims:

This listing of claims will replace all prior versions and listings, of claims in the application:

- 1 1. (Amended) A method of copper metallization in the fabrication of an integrated circuit device comprising:
 - 3 providing an opening through a dielectric layer overlying a substrate on a wafer;
 - 4 forming a copper layer to completely fill said opening;
 - 5 forming a buffer zone on a surface of said copper layer by exposing said copper
 - 6 layer to an NF₃ plasma; and
 - 7 depositing a capping layer overlying said copper layer and said buffer zone to complete said copper metallization in said fabrication of said integrated circuit device.
- 1 2. (Original) The method according to Claim 1 further comprising forming semiconductor device structures in and on said substrate wherein said semiconductor device structures include gate electrodes, source/drain regions, and lower level metallization.
- 1 3. (Original) The method according to Claim 2 wherein said opening is made to one of said semiconductor device structures within said substrate.
- 1 4. (Original) The method according to Claim 1 wherein said depositing said capping layer is an in-situ process.
- 1 5. (Original) The method according to Claim 1 wherein said step of forming said copper layer is selected from the group consisting of: physical vapor deposition, chemical vapor deposition, electroplating, and electroless plating.

1 6. (Amended) The method according to Claim 1 wherein said step of forming
2 ~~a~~ said buffer zone comprises applying ~~F ions or~~ controlled corrosion gas to said copper
3 surface.

1 7. (Original) The method according to Claim 1 wherein said capping layer is
2 selected from the group consisting of silicon nitride and silicon carbide and wherein said
3 capping layer has a thickness of between about 200 and 1000 Angstroms.

1 8. (Amended) A method of copper metallization in the fabrication of an
2 integrated circuit device comprising:

3 providing an opening through a dielectric layer overlying a substrate on a wafer;
4 forming a copper layer to completely fill said opening; and
5 applying ~~F ions to~~ treating said copper layer with NF₃ plasma to form a buffer
6 zone on a surface of said copper layer and in-situ depositing a capping layer overlying
7 said copper layer to complete said copper metallization in said fabrication of said
8 integrated circuit device.

1 9. (Original) The method according to Claim 8 further comprising forming
2 semiconductor device structures in and on said substrate wherein said semiconductor
3 device structures include gate electrodes, source/drain regions, and lower level
4 metallization.

1 10. (Original) The method according to Claim 9 wherein said opening is made
2 to one of said semiconductor device structures within said substrate.

1 11. (Original) The method according to Claim 8 wherein said step of forming
2 said copper layer is selected from the group consisting of: physical vapor deposition,
3 chemical vapor deposition, electroplating, and electroless plating.

1 12. (Cancelled)

1 13. (Original) The method according to Claim 8 herein said capping layer is
2 selected from the group consisting of silicon nitride and silicon carbide and wherein said
3 capping layer has a thickness of between about 200 and 1000 Angstroms.

1 14. (Amended) A method of copper metallization in the fabrication of an
2 integrated circuit device comprising:

3 providing an opening through a dielectric layer overlying a substrate on a wafer;
4 forming a copper layer to completely fill said opening wherein copper oxide forms
5 naturally on a surface of said copper layer; and
6 applying a gas containing F ions to said copper layer wherein said F ions remove
7 said copper oxide and form a buffer zone on a surface of said copper layer and in-situ
8 depositing a capping layer overlying said copper layer to complete said copper
9 metallization in said fabrication of said integrated circuit device.

1 15. (Original) The method according to Claim 14 further comprising forming
2 semiconductor device structures in and on said substrate wherein said semiconductor
3 device structures include gate electrodes, source/drain regions, and lower level
4 metallization.

1 16. (Original) The method according to Claim 15 wherein said opening is
2 made to one of said semiconductor device structures within said substrate.

3 17. (Original) The method according to Claim 14 wherein said step of forming
4 said copper layer is selected from the group consisting of: physical vapor deposition,
5 chemical vapor deposition, electroplating, and electroless plating.

1 18. (Amended) The method according to Claim 14 wherein said step of
2 applying a gas containing F ions to said copper layer comprises treating said copper
3 with NF₃ plasma.

1 19 (Original) The method according to Claim 14 wherein said buffer zone
2 transfers thermal vertical strain in said copper to horizontal strain thereby preventing
3 formation of copper hillocks.

1 20. (Original) The method according to Claim 14 wherein said capping layer is
2 selected from the group consisting of silicon nitride and silicon carbide and wherein said
3 capping layer has a thickness of between about 200 and 1000 Angstroms.